Remarks

The description in the Background section of the specification appearing on page 1 of the specification is clarified in response to the objection raised at page 2, Item 5 of the Official Action.

Several objection and rejections under the first and second paragraphs of 35 USC §112 were set forth at pp. 2-5 of the Official Action, arising from applicant's introduction of the terms "a single I/O request" and "multitask" in the previous response. By the present amendment, those terms are removed from the present claims, thereby to obviate those objections and rejections.

In response to the position taken in the Official Action that the specification does not describe or enable the execution of a single I/O request by multiple simultaneous processes, applicant respectfully disagrees. For example, at least the passages discussed above on page 1 of the specification do provide support for such a technique.

In any case, the rejections made on this basis are obviated by the present amendments to the claims, which delete reference to any "single" I/O request. Those amendments, however, do not constitute an acquiescence by the applicant as to the propriety of the rejections, because the claims continue to cover embodiments in which the simultaneously performed I/O processes may relate to plural I/O requests, a single I/O request, or both

(see p. 1 of the specification). What is more significant in the present claims is not whether it is a single or plural I/O requests that are being processed, but rather that the recited multitasks are all of the same type - i.e., I/O processes executed to carry out an I/O request to the disk array.

Claims 1-7, 9 and 10 were rejected as unpatentable over O'NEIL et al. 6,085,287, JOHNSON et al. 6,308,245 and RYAN 5,367,656. Claims 5 and 10 were further rejected as being unpatentable over O'NEIL et al., JOHNSON et al. and RYAN further in view of HORII et al. JP 08-077025A. Those rejections are respectfully traversed, for the following reasons.

The claims as amended herewith specify that both the high and low priority tasks are I/O processes to a disk array. Performance is improved by executing in parallel only a fixed number (or fewer) of high priority processes provided the cache hit ratio is above a certain level, and increasing the number of I/O processes executed in parallel to include low priority processes only when the cache hit ratio drops below that level.

The Official Action acknowledges that O'NEIL et al. and JOHNSON et al. do not disclose limiting the number of higher priority tasks when the cache hit ratio is above a prescribed value. The Official Action relies on RYAN for the suggestion to modify these references to include this feature.

However, RYAN merely discloses that a miss prediction operation is halted when the cache hit ratio is above a threshold

and that the regular cache accessing continues. These two operations (miss prediction and regular cache accessing) are separate operations that are dissimilar and not I/O processes that are generated for processing I/O requests to a disk.

The amended claims are now more explicit in reciting that both the high priority and low priority tasks according to the invention are I/O processes generated from I/O requests to a disk array. This further distinguishes the claims from RYAN not only in that both priority tasks are now more clearly required to be of the same type, but also in that this same type of process is distinct from either type of process (miss prediction and regular cache accessing) described by RYAN.

The amended claim language is further distinct over RYAN and the other applied prior art in specifying that the I/O requests and processes pertain to I/O operations performed on the disk array. Of course, any accessing of cache memory might be considered to constitute an I/O operation in a general sense, and the claims as amended herewith now more clearly avoid any such overbroad reading. Indeed, the miss prediction and regular cache accessing operations described by RYAN are more in the nature of housekeeping programs that would be stored, for example, in the local memory 33 and processor cache 32 of the embodiment of present Fig. 1, rather than I/O processes to the disk array that therefore ultimately involve the disk cache memory 22 and/or the disk I/F control portion 23 of that embodiment. Thus, the

technique of the present invention differs fundamentally from the disclosure of RYAN and the other references applied in combination therewith, and the claims as amended herewith are believed now better to reflect those differences.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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